IN THE CLAIMS:

Please amend the claims as set forth below:

1. (Currently Amended) A processor comprising:

a register configured to store a mask comprising a plurality of indications, wherein each of the plurality of indications corresponds to a respective one of a plurality of flags;

an execution core coupled to the register, wherein the execution core is configured, in response to a system call instruction, to ~~selectively~~ conditionally update a given flag of the plurality of flags ~~responsive to~~ dependent on a respective indication of the plurality of indications in the mask; and

a second register configured to store the plurality of flags, wherein the execution core is configured to store the updated plurality of flags in the second register in response to the system call instruction.

2. (Original) The processor as recited in claim 1 wherein the execution core is configured to update a first flag of the plurality of flags in response to the corresponding indication in the mask being in a first state and wherein the execution core is configured to retain a current state of the first flag in response to the corresponding indication in the mask being in a second state.

3. (Original) The processor as recited in claim 2 wherein the execution core is configured to update the first flag by clearing the first flag.

4. (Original) The processor as recited in claim 3 wherein the corresponding indication is a bit.

5. (Original) The processor as recited in claim 4 wherein the first state comprises the bit being set.

6. (Currently Amended) The processor as recited in claim 1 wherein the execution core is coupled to receive an indication of an operating mode of the processor, and wherein the execution core is configured to ~~selectively~~ conditionally update the given flag in a first operating mode, and wherein the execution core is configured not to perform a ~~selective~~ conditional update in a second operating mode.

7. (Original) The processor as recited in claim 6 wherein the execution core is configured to perform a predetermined update of the plurality of flags in the second operating mode.

8. (Cancelled)

9. (Currently Amended) An apparatus comprising:

a storage location configured to store a mask comprising a plurality of indications, wherein each of the plurality of indications corresponds to a respective one of a plurality of flags;

a processor coupled to the storage location, wherein the processor is configured, in response to a system call instruction, to ~~selectively~~ conditionally update a given flag of the plurality of flags ~~responsive to~~ dependent on a respective indication of the plurality of indications in the mask; and

a second storage location configured to store the plurality of flags, wherein the processor is configured to store the updated plurality of flags in the second storage location in response to the system call instruction.

10. (Original) The apparatus as recited in claim 9 wherein the processor is configured to update a first flag of the plurality of flags in response to the corresponding indication in

the mask being in a first state and wherein the processor is configured to retain a current state of the first flag in response to the corresponding indication in the mask being in a second state.

11. (Original) The apparatus as recited in claim 10 wherein the processor is configured to update the first flag by clearing the first flag.

12. (Original) The apparatus as recited in claim 11 wherein the corresponding indication is a bit.

13. (Original) The apparatus as recited in claim 12 wherein the first state comprises the bit being set.

14. (Currently Amended) The apparatus as recited in claim 9 wherein the processor is configured to ~~selectively~~ conditionally update the given flag in a first operating mode, and wherein the processor is configured not to perform a ~~selective~~ conditional update in a second operating mode.

15. (Original) The apparatus as recited in claim 14 wherein the processor is configured to perform a predetermined update of the plurality of flags in the second operating mode.

16. (Cancelled)

17. (Currently Amended) A method comprising processing a system call instruction, the processing comprising ~~selectively~~ conditionally updating a given flag of a plurality of flags ~~responsive to~~ dependent on a corresponding indication in a mask, wherein the mask comprises a plurality of indications, and wherein each of the plurality of indications corresponds to a respective flag of the plurality of flags and indicates whether or not the respective flag is updated in response to the system call instruction; and the processing further comprising storing the updated plurality of flags in a storage location configured to store the plurality of flags.

18. (Currently Amended) The method as recited in claim 17 wherein the ~~selectively~~ conditionally updating comprises:

updating a first flag of the plurality of flags in response to a first state of the corresponding indication; and

retaining a current state of the first flag in response to a second state of the corresponding indication.

19. (Original) The method as recited in claim 18 wherein the updating the first flag comprises clearing the first flag.

20. (Currently Amended) The method as recited in claim 17 wherein the ~~selectively~~ conditionally updating is performed in a first operating mode, and wherein the ~~selectively~~ conditionally updating is not performed in a second operating mode.

21. (Original) The method as recited in claim 20 further comprising performing a fixed update of the plurality of flags in the second operating mode.

22. (Previously Presented) A processor comprising:

a register configured to store a value that defines which flags of a plurality of flags are to be cleared in response to a system call instruction and which flags of the plurality of flags are to be preserved in response to the system call instruction;

an execution core coupled to the register, wherein the execution core is configured, in response to the system call instruction, to clear one or more selected flags of a plurality of flags and preserve one or more other flags of the plurality of flags responsive to the value in the register; and

a second register configured to store the plurality of flags, wherein the execution core is configured to store the updated plurality of flags in the second register in response to the system call instruction.

23-24. (Cancelled)

25. (Previously Presented) The processor as recited in claim 22 wherein the execution core is coupled to receive an indication of an operating mode of the processor, and wherein the execution core is configured to clear one or more selected flags and preserve one or more other flags in a first operating mode.

26. (Previously Presented) The processor as recited in claim 25 wherein the execution core is configured to perform a predetermined update of the plurality of flags in a second operating mode.

27. (Cancelled)

28. (Previously Presented) An apparatus comprising:

a storage location configured to store a value that defines which flags of a plurality of flags are to be cleared in response to a system call instruction and which flags of the plurality of flags are to be preserved in response to the system call instruction;

a processor coupled to the storage location, wherein the processor is configured, in response to the system call instruction, to clear one or more selected flags of a plurality of flags and preserve one or more other flags of the plurality of flags responsive to the value in the storage location; and

a second storage location configured to store the plurality of flags, wherein the

processor is configured to store the updated plurality of flags in the second storage location in response to the system call instruction.

29-30. (Cancelled)

31. (Previously Presented) The apparatus as recited in claim 28 wherein the processor is configured to operate according to an operating mode, and wherein the processor is configured to clear one or more selected flags and preserve one or more other flags in a first operating mode.

32. (Previously Presented) The apparatus as recited in claim 31 wherein the processor is configured to perform a predetermined update of the plurality of flags in a second operating mode.

33. (Cancelled)

34. (Previously Presented) A computer accessible medium storing a plurality of instructions which, when executed in response to a system call instruction, clear one or more selected flags of a plurality of flags and preserve one or more other flags of the plurality of flags responsive to a value in a storage location, wherein the value defines which flags of the plurality of flags are to be cleared in response to a system call instruction and which flags of the plurality of flags are to be preserved in response to the system call instruction, and wherein the plurality of instructions, when executed, store the updated plurality of flags in a second storage location in response to the system call instruction.

35-36. (Cancelled)

37. (Previously Presented) The computer accessible medium as recited in claim 34 wherein the plurality of instructions, when executed in a first operating mode, clear the one or more selected flags and preserve the one or more other flags, and wherein the

plurality of instructions, when executed in a second operating mode perform a predetermined update of the plurality of flags.

38. (Cancelled)

39. (Previously Presented) The computer accessible medium as recited in claim 34 wherein the value in the storage location comprises a mask having a respective indication for each of the plurality of flags.